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SHEET 1 OF 1

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| INFORMATION DISCLOSURE CITATION PTO-1449 | 26615 PATENT TRADEMARK OFFICE | ATTORNEY'S DKT No. H1505 | APPLICATION No. Unassigned | |
| | | APPLICANT(S) Bin YU et al. | | |
| | | FILING DATE September 3, 2003 | GROUP Unassigned | |

| U.S. PATENT DOCUMENTS | | | | | | |
|------------------------|------------|------|------|-------|----------|----------------|
| EXAMINER'S INITIALS | PATENT NO. | DATE | NAME | CLASS | SUBCLASS | FILING DATE |
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| FOREIGN PATENT DOCUMENTS | | | | | | | |
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| EXAMINER'S INITIALS | PATENT NO. | DATE | COUNTRY | CLASS | SUBCLASS | Translation | |
| | | | | | | Yes | No |
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| OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) | |
|--|---|
| <i>See</i> | Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325. |
| <i>See</i> | Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424. |
| | Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886. |
| | Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70. |
| <i>See</i> | Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27. |

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| EXAMINER <i>Debra Kuyper</i> | DATE CONSIDERED <i>8/30/05</i> |
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).